Jiwaji University
SOS in Computer Science and Applications
B.C.A. (IV Semester)
Paper -402 Advance Computer Architecture
Unit 2

Topic:

SEMI CONDUCTOR / MAIN MEMORY
CHIP PACKAGING ERROR CORRECTION

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RAM (Random Access Memory)

Random access memory (RAM) is the best known form of computer memory. RAM is considered "random access" because you can access any memory cell directly if you know the row and column that intersect at that cell.

Types of RAM:-

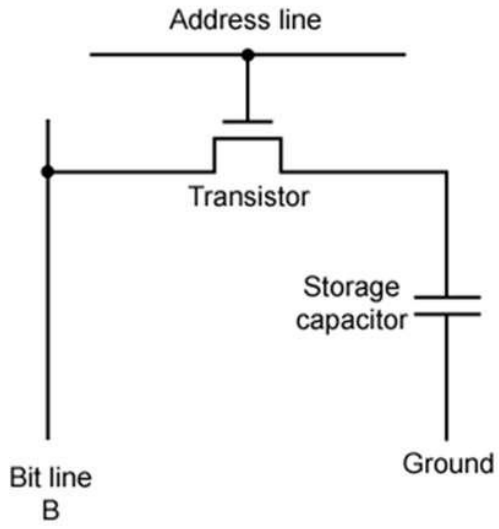
•Static RAM (SRAM)

•Dynamic RAM (DRAM)

Types of RAM

• **Dynamic RAM (DRAM)** – are like leaky capacitors; initially data is stored in the DRAM chip, charging its memory cells to maximum values. The charge slowly leaks out and eventually would go to low to represent valid data; before this happens, a **refresh** circuitry reads the contents of the DRAM and rewrites the data to its original locations, thus restoring the memory cells to their maximum charges.

–Each cell stores bit with a capacitor and transistor.
–Large storage capacity
–Needs to be refreshed frequently.
–Used to create main memory.
–Slower and cheaper than SRAM.



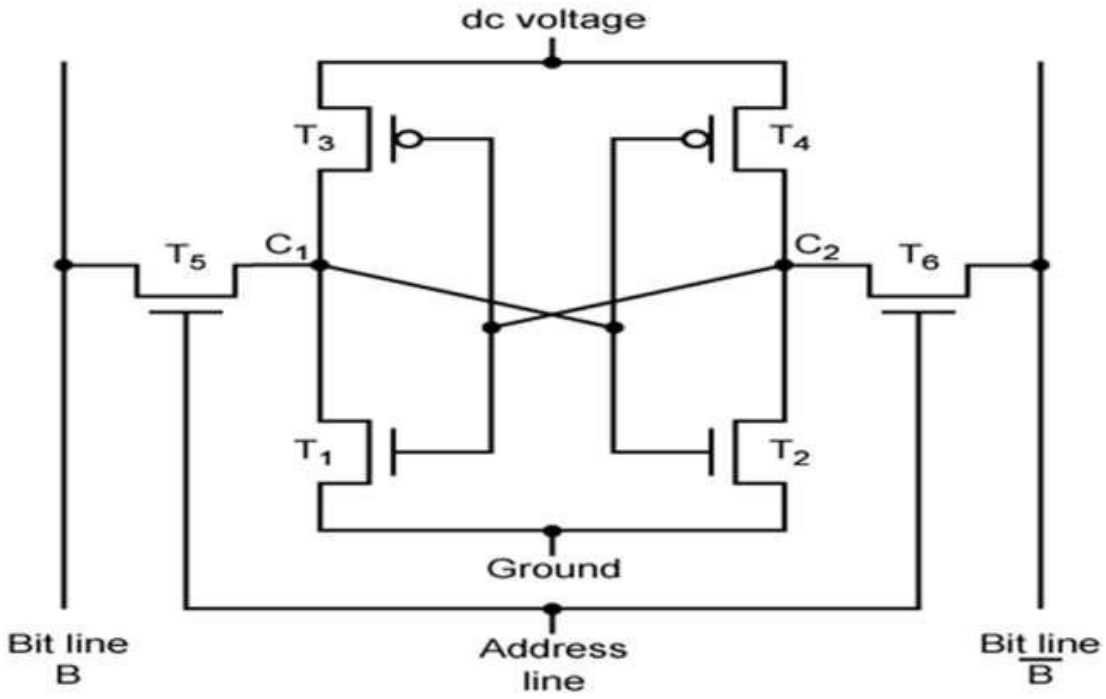
• **Static RAM (SRAM)** – is more like a register; once the data has been written, it will stay valid, it doesn't have to be refreshed. Static RAM is faster than DRAM, also more expensive. Cache memory in PCs is constructed from SRAM memory

– a bit of data is stored using the state of a flip-flop.

–Retains value indefinitely, as long as it is kept powered.

–Mostly uses to create cache memory of CPU.

–Faster and more expensive than DRAM.



Static RAM

- Uses flip flop to store information
- Needs more space
- Faster, digital device
- Expensive, big in size
- Don't require refreshing circuit
- Used in cache memory

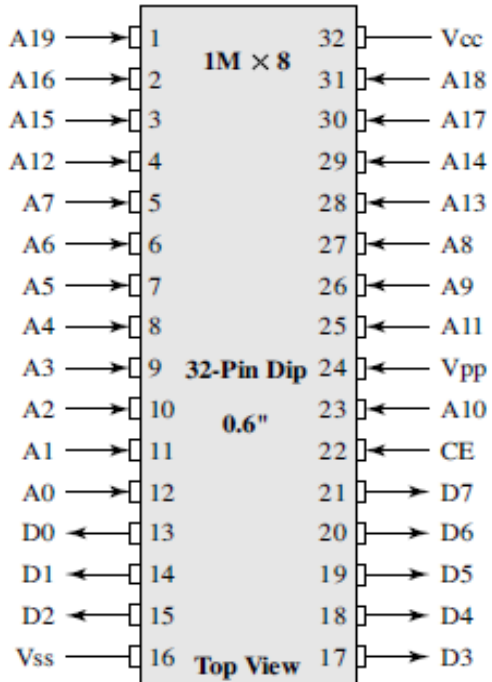
Dynamic RAM

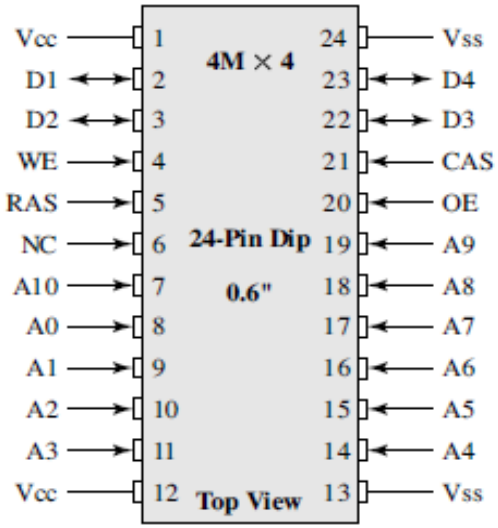
- Uses capacitor to store information
- More dense i.e. more cells can be accommodated per unit area
- Slower, analog device
- Less expensive, small in size
- Needs refreshing circuit
- Used in main memory, larger memory units

Chip Packaging

As was mentioned in Chapter 2, an integrated circuit is mounted on a package that contains pins for connection to the outside world. an example EPROM package, which is an 8-Mbit chip organized as 1M 8. In this case, the organization is treated as a one-word-per-chip package. The package includes 32 pins, which is one of the standard chip package sizes. The pins support the following signal lines:

• The address of the word being accessed. For 1M words, a total of 20 (220 1M) pins are needed (A0–A19).
• The data to be read out, consisting of 8 lines (D0–D7).
• The power supply to the chip (Vcc).
• A ground pin (Vss). • A program voltage (Vpp) that is supplied during programming (write operations).
• A chip enable (CE) pin. Because there may be more than one memory chip, each of which is connected to the same address bus, the CE pin is used to indicate whether or not the address is valid for this chip.The CE pin is activated by logic connected to the higher-order bits of the address bus (i.e., address bits above A19).The use of this signal is illustrated presently.





Error Correction

•A semiconductor memory is subject to errors. 2 categories:

•Hard Failure

–Permanent physical defect so that the memory cell/cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1. Hard errors can be caused by harsh environmental abuse, manufacturing defects, and wear.

•Soft Error

–Random, non-destructive events that alters the contents of one or memory cells.

–No permanent damage to memory.

–Can be caused by power supply problem.

• Both are not desirable, and most modern main memory have systems include logic for both detecting and correcting errors.

•The simplest of the error-correcting codes is the Hamming code.

Error Correction: Error-Correcting Code Function

1. When data are to be read into memory, a calculation depicted as a function f is performed on the data to produce a code.
2. Both the code and the data are stores, thus if an M-bit word of data is to be stored, and the code is of length K bits, then the actual size of the stored word in M + K bits.
3. When the previously stored word is read out, the code is used to detect and possibly correct errors.

4. A new set of K code bits is generated from the M data bits and compared with the fetched bits.

5. The comparison yields one of the 3 results:

–No errors are detected. The fetched data bits are sent out.

–An error is detected, and it is possible to correct the error. The data bits plus error correction bits are fed into a corrector, which produces a corrected set of M bits to be sent out.

–An error is detected, but it is not possible to correct it. This condition is reported.

6. A code is characterized by the number of bits errors in a word that it can correct and detect.